IN THE SPECIFICATION

In the Title of the Invention, please make the following change:

~~SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE~~ SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH DUMMY BUMPS

Please amend the paragraph beginning at page 1, line 8 as follows:

Particularly, the invention relates to a semiconductor integrated circuit device provided with the facedown bonding bumps having an electrical connection capability that are provided at a terminal section on the surface of a semiconductor substrate and which has electrically-non-connected dummy bumps.

Please amend the paragraph beginning at page 1, line 22 as follows:

For theses reasons, a semiconductor integrated circuit device has been conventionally packaged as a chip without performing plastic sealing. Therefore, a method ~~it~~ has been adopted ~~a method~~ for providing projections, such as known for bumps, on the terminals of a chip and mounting the chip to a substrate by a flip chip bonding method. Specifically, when a semiconductor integrated circuit device is packaged, facedown bonding is adopted for placing a chip opposite an object of connection, such as a substrate, and pressing the chip directly on the substrate using anisotropic conductive particles (ACP) or a conductive material.

Please amend the paragraph beginning at page 1, line 33 as follows:

In this case, since the back side of the chip is ground ~~from~~ due to a need ~~of~~ for slimming down a chip, the chip comes to be warped or susceptible to variations in its thickness, and furthermore the horizontal positions of the bumps formed on the surface of the chip are also displaced (see Fig. ~~7A~~ 7(a))

Please amend the paragraph beginning at page 2, line 2 as follows:

In such an occasion, one of the four corners of the chip often comes into contact with the substrate at first prior to the rests of the corners doing in the facedown mounting because of

fluctuations in the height of bumps or the insufficient precision of a bonding machine used for bonding a chip on the mounting substrate (see Fig. ~~7B~~ 7(b)).

Please amend the paragraph beginning on page 2, at line 21 as follows:

Furthermore, JP-A-7-263488 discloses the dummy bumps~~;~~ . ~~h~~However, the dummy bumps are not used for the purpose of the facedown bonding, ~~on the top of this~~ and besides, there is no idea of solving the problems such as the chip being warped or susceptible to variations in its thickness or subjected to the heavier load stress.

Please amend the paragraph beginning on page 2, at line 27 as follows:

In recent years, because of an improvement in performance of an LSI; particularly, due to colorization of an LCD driver or a tendency of the larger size of a screen, the numbers of the terminals to be used are increased, and a highly-integrated semiconductor process is required. In such an occasion, downsize of a chip area cannot be achieved unless intervals between bumps are made narrower than they have been made before. In ~~reflection~~ recognition of this requirement, the area of each bump also comes to be smaller, which ended up increasing the number of dummy bumps to be disposed at each of the corners of one chip.

Please amend the paragraph beginning on page 3, at line 6 as follows:

In contrast, the areas of the individual bumps are required to be substantially the same in size with each other from a need of electrically connecting the chip with the substrate in use of the ACP. As a result, as shown in Fig. 8, each of the respective bumps in case of narrowing the interval between the bumps might become a narrow shape. For these reasons, as the numbers of the dummy bumps increase, the so-called ~~an~~ invalid area (hatched in Fig. 8), a space residing between the bumps, becomes larger in the ratio of the bump area. Accordingly, an increase in the number of dummy bumps merely results in increase of the area where the dummy bumps are disposed in relation to the total area of the bumps, which becomes a limitation on downsizing of a chip.

Please amend the paragraph beginning on page 3, at line 19 as follows:

Reflecting these requirements, in the related art, the following ~~kind of the way~~ has been adopted. Fig. 1 is a view showing the entirety of a chip of a semiconductor integrated circuit device to be used for facedown bonding of the related art. The semiconductor integrated circuit device chip 1 has facedown bonding bumps 6 arranged so as to surround an unillustrated internal circuit. In the embodiment, bumps are arranged along four sides of a chip 1 of the semiconductor integrated circuit device surrounding the internal circuit. In an alternative configuration, no bumps 6 are provided along one or two specific edges, and a circuit or wiring is provided instead of the bumps.

Please amend the paragraph beginning on page 3, at line 31 as follows:

Figs. 2~~,~~ is an enlarged view showing a chip corner section 5 enclosed by broken edges in Fig. 1 as a representative of four corners of the semiconductor integrated circuit device chip 1. The drawings will be described herein below.

Please amend the paragraph beginning on page 4, at line 9 as follows:

However, this related art is still not sufficient ~~level~~ for overcoming the above-mentioned problems from the aspects of the recent improvement functionalities of LSI technologies or highly advanced semiconductor integration processes.

Please amend the paragraph beginning on page 4, at line 33 as follows:

Having said bump arrangement, an area located between the dummy bumps, which is regarded as an open space, can also be used as an area for dummy bumps. As a result, the area on the semiconductor chip to be used for placing dummy bumps becomes smaller than that ~~of being~~ required in the related art. Hence, the area of the semiconductor chip can be made small.

Please amend the paragraph beginning on page 5, at line 3 as follows:

The semiconductor integrated circuit device according to the second aspect of this invention is characterized by the semiconductor integrated circuit device of the first aspect, and further comprising a wiring which is disposed below the dummy bumps with at least one insulating film in-between and ~~is~~ not electrically connected to the dummy bumps.

Please amend the paragraph beginning on page 6, at line 10 as follows:

Fig. 3 is a bump layout view showing the first embodiment. There are provided the circuit connection bumps 3 connected to the unillustrated internal circuit, and one dummy bump 2a which is placed for each edge, between the corner section of the chip 1 of the semiconductor integrated circuit device and the bumps 3. The area of the dummy bump 2a is approximately double that of the circuit connection bump 3. There can be obtained a load capacity effect of an area corresponding to the area occupied by a total of four circuit connection bumps 3. The inside of the area enclosed by broken lines corresponds to the are on the chip 1 of the semiconductor integrated circuit device, which is ~~ensured~~ reserved for dummy bumps. A load capacity effect which is identical with that of being achieved by the layout of the related-art bumps as sown in Fig. 2 can be achieved by the layout of the related-art bumps as shown in Fig. 2 can be achieved by the bump layout occupying a much smaller area.

Please amend the paragraph beginning on page 6, at line 10 as follows:

Fig. 3 is a bump layout view showing the first embodiment. There are provided the circuit connection bumps 3 connected to the unillustrated internal circuit, and one dummy bump 2a which is placed for each edge, between the corner section of the chip 1 of the semiconductor integrated circuit device and the bumps 3. The area of the dummy bump 2a is approximately double that of the circuit connection bump 3. There can be obtained a load capacity effect of an area corresponding to the are occupied by a total of four circuit connection bumps 3. The inside of the are enclose by broken lines corresponds to the area on the chip 1 of the semiconductor integrated circuit device, which is ~~ensured~~ [reserved] for dummy bumps. A load capacity effect which is identical with that of being achieved by the layout of the related-art bumps as sown in Fig. 2 can be achieved by the bump layout occupying a much smaller area.

Please amend the paragraph beginning on page 6, at line 25 as follows:

Fig. 4 is a bump layout view showing a second embodiment. There are provided the circuit connection bumps 3 connected to the unillustrated internal circuit, and one dummy bump 2b which is placed at the corner section of the chip 1 of the semiconductor integrated circuit device and assumes a shape, the shape avoiding a circuit wiring 4 and not being rectangular. The

area of the dummy bump 2b is four times or more that of the circuit connection bump 3. For this reason, there can be obtained a load capacity effect large than that obtained from the area occupied by the four circuit connection bumps 3. The inside of the area enclosed by broken line corresponds to the area on the chip 1 of the semiconductor integrated circuit device, which is ~~ensured~~ reserved for dummy bumps. A load capacity effect which is identical with that of being achieved by the first embodiment as shown in Fig. 3 is achieved by the bump layout occupying a much smaller area.

Please amend the paragraph beginning on page 7, at line 5 as follows:

Fig. 5 is a view showing a third embodiment. There are provided the circuit connection bumps 3 connected to the unillustrated internal circuit, and one rectangular dummy bump 2c which is placed at the corner section of the chip 1 of the semiconductor integrated circuit wiring portion 4. Since there area of the dummy bump 2c is larger than that of the dummy bump 2b of the second embodiment shown in Fig. 4, there can be obtained a load capacity effect which is much greater than that ~~of being~~ achieved in the second embodiment as shown in Fig. 4.

Please amend the paragraph beginning on page 7, at line 15 as follows:

The load capacity effect achieved when the facedown bonding dummy bumps of the invention are formed on the chip will now be described by references to Figs. 6~~A~~ (a) and 6~~B~~ (b). Fig. 6~~A~~ (a) is a front view showing a positional relationship between typical bumps and dummy bumps on a chip, in which a normal bump width is denoted by "a", a bump space by "b", a dummy bump width by "c", and a distance from the dummy bump to the chip edge by "d". For instance, in Fig. 6~~A~~ (a), when these values are assumed such as a=30, b=20, d=20 and e=100, a graph A in Fig. 6~~B~~ (b) shows an example of an increasing area of dummy bumps when the numbers of dummy bumps, each width of the dummy bumps being the same as that of normal bump, are increased stepwisely in the manner of one, two, three, ... while a graph B (this invention) shows the other example when the width of the dummy bump is expanded freely without increasing the number of the dummy bump. As can be seen from the graph, the load capacity effect of the dummy bump can be remarkably improved by increasing thea are of the dummy bumps ~~in~~ linearly or gradually without allowing the chip area to be increased accordingly.

Please amend the paragraph beginning on page 7, at line 34 as follows:

According to a semiconductor integrated circuit device of the invention, dummy bumps having a larger area than that of the circuit connection bumps, which are connected to an internal circuit, can be implemented in an area on a chip of a semiconductor integrated circuit device of which the area ~~is~~ to be ~~ensured~~ reserved for dummy bumps ~~that~~ is smaller than the related-art dummy bumps. In this way, a load capacity effect which is equal to or greater than that of being imposed on the area of a related-art ship can be made on the chip area that is smaller than that of the related-art chip.